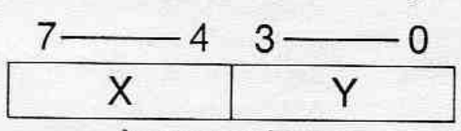
Mnemonic	Bytes	Cycles	Description of Operation
LDAX D	1	2	(A) ← [(D) (E)] Load the accumulator with the content of memory location addressed by the content of register D and E.
INX B	1	1	(B) (C) ← (B) (C) + 1 The content of register pair B and C is incremented by one. All of the condition flip-flops are not affected.
INX H	1	1	(H) (L) ← (H) (L) + 1 The content of register H and L is incremented by one. All of the condition flip-flops are not affected.
INX D	1	1	(D) (E) ← (D) (E) + 1
INX SP	1	1	(SP) ← (SP) + 1
DCX B	1	1	(B) (C) ← (B) (C) − 1
DCX H	1	1	(H) (L) ← (H) (L) − 1
DCX D	1	1	(D) (E) ← (D) (E) − 1
DCX SP	1	1	(SP) ← (SP) − 1
CMA	1	1	(A) ← $\overline{(A)}$ The content of accumulator is complemented. The condition flip-flops are not affected.
STC	1	1	(Carry) ← 1 Set the carry flip-flop to 1. The other condition flip-flops are not affected.
CMC	1	1	(carry) ← $\overline{(carry)}$ The content of carry is complemented. The other condition flip-flops are not affected.

DAA	1	1	Decimal Adjust Accumulator
			The 8-bit value in the accumulator containing the result from an arithmetic operation on decimal operands is adjusted to contain two valid BCD digits by adding a value according to the following rules:
			 
			
			If (Y ≥ 10) or (carry from bit 3) then Y = Y + 6 with carry to X digit.
			If (X ≥ 10) or (carry from bit 7) or [(Y ≥ 10) and (X = 9)] then X = X + 6 (which sets the carry flip-flop).
			Two carry flip-flops are used for this instruction. CY_1 represents the carry from bit 3 (the fourth bit) and is accessible as a fifth flag. CY_2 is the carry from bit 7 and is the usual carry bit.
			All condition flip-flops are affected by this instruction.

SHLD <B_2> <B_3>	3	5	[<B_3> <B_2>] ← (L), [<B_3> <B_2> + 1] ← (H) Store the contents of registers H and L into the memory location addressed by byte two and byte three of the instructions.
LHLD <B_2> <B_3>	3	5	(L) ← [<B_3> <B_2>], (H) ← [<B_3> <B_2> + 1] Load the registers H and L with the contents of the memory location addressed by byte two and byte three of the instruction.
EI	1	1	Interrupt System Enable
DI	1	1	Interrupt System Disable The Interrupt Enable flip-flop (INTE) can be set or reset by using the above mentioned instructions. The INT signal will be accepted if the INTE is set. When the INT signal is accepted by the CPU, the INTE will be reset immediately. During interrupt enable or disable instruction executions, an interrupt will not be accepted.
INR M	1	3	[M] ← [M] + 1. The content of memory designated by registers H and L is incremented by one. All of the condition flip-flops except carry are affected by the result.
DCR M	1	3	[M] ← [M] − 1. The content of memory designated by registers H and L is decremented by one. All of the condition flip-flops except carry are affected by the result.