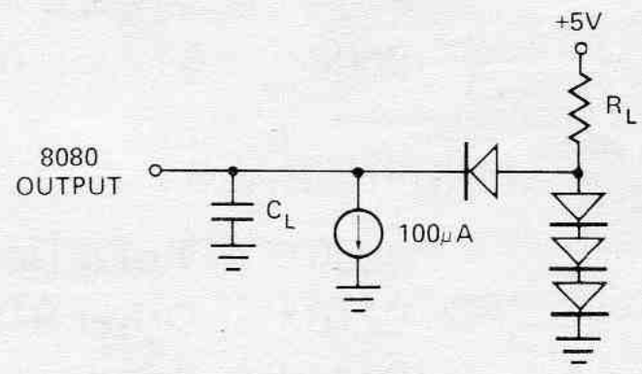
A.C. CHARACTERISTICS (Continued)

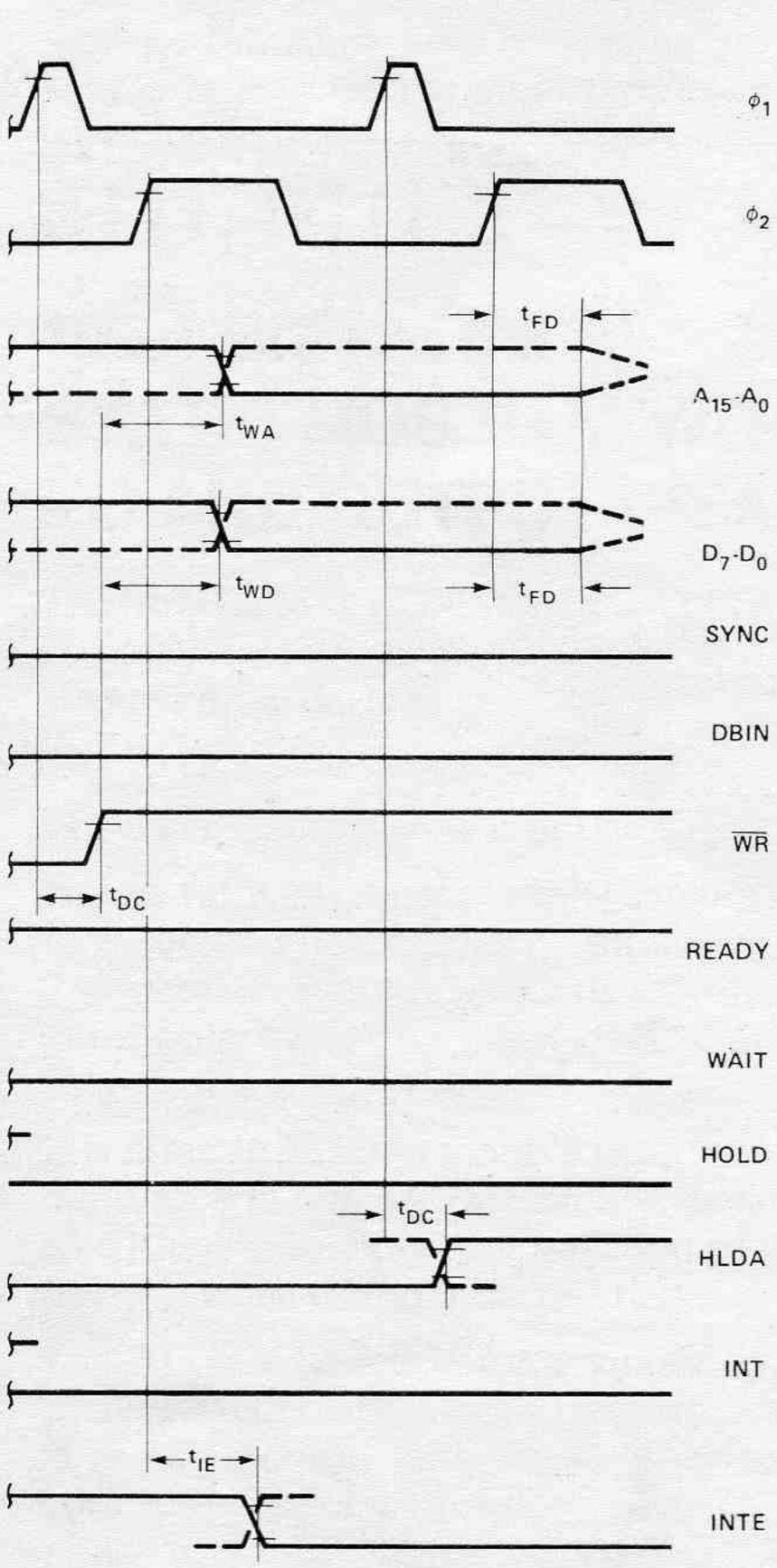
$T_A = 0°C$ to $70°C$, $V_{DD} = +12V \pm 5\%$, $V_{CC} = +5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, $V_{SS} = 0V$, Unless Otherwise Noted

Symbol	Parameter	Min.	Max.	Unit	Test Condition
t_{DS2}	Data "Setup Time" to ϕ_2 During DBIN	150		nsec	$R_L = 4.5k\Omega$, $C_L = 50pf$
t_{DH} [1]	Data "Hold Time" From ϕ_2 During DBIN	t_{DF}		nsec	
t_{IE} [2]	INTE Output Delay From ϕ_2		200	nsec	
t_{RS}	Ready "Setup Time" During ϕ_2	120		nsec	
t_{HS}	Hold "Setup Time" to ϕ_2	140		nsec	
t_{IS}	INT "Setup Time" During ϕ_2 (During ϕ_1 in Halt Mode)	180		nsec	
t_H	"Hold Time" From ϕ_2 (Ready, INT, Hold)	0		nsec	
t_{FD}	Delay to Float During Hold (Address and DATA BUS)		120	nsec	
t_{WA} [2]	Address Stable From $\overline{WR}$	t_{D3}		nsec	$R_L = 4.5k\Omega$, $C_L = 100pf$
t_{AW} [2]	Address Stable Prior to $\overline{WR}$	[5]		nsec	$R_L = 4.5k\Omega$, $C_L = 100pf$
t_{WD} [2]	Output Data Stable From $\overline{WR}$	t_{D3}		nsec	$R_L = 2.1k\Omega$, $C_L = 100pf$
t_{DW} [2]	Output Data Stable Prior to $\overline{WR}$	[6]		nsec	$R_L = 2.1k\Omega$, $C_L = 100pf$

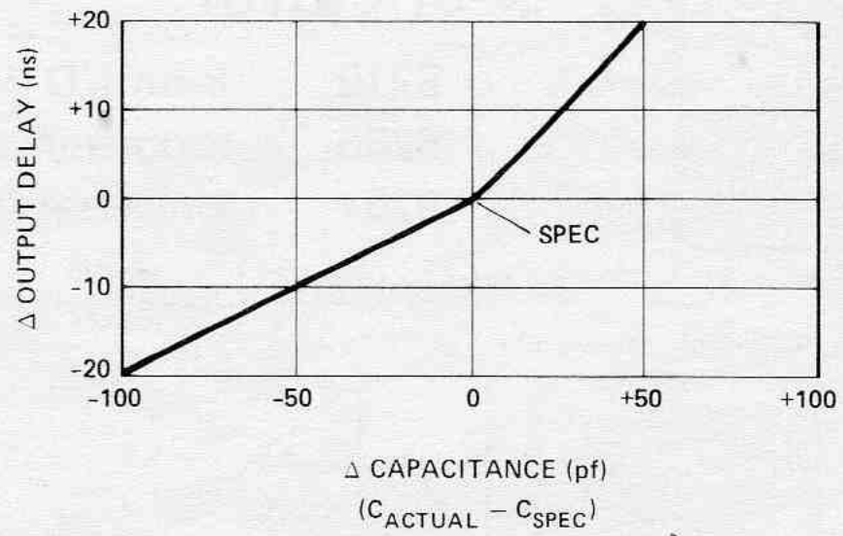
NOTES: 1. Data input should be enabled with DBIN status. No bus conflict can then occur and data hold time is assured.
2. Load circuit



3. $t_{CY} = t_{D3} + t_{r\phi2} + t_{\phi2} + t_{f\phi2} + t_{D2} + t_{r\phi1} \geq 480ns$.



TYPICAL Δ OUTPUT DELAY VS. Δ CAPACITANCE



4. The following are relevant when interfacing the 8080 to devices having $V_{IH} = 3.3V$:
   a) Maximum output rise time from .8V to 3.3V = 140ns @ C_L = SPEC.
   b) Output delay when measured to 3.0V = SPEC + 60ns @ C_L = SPEC.
   c) If $C_L \neq$ SPEC add .6ns/pf if $C_L > C_{SPEC}$, subtract .3ns/pf (from modified delay) if $C_L < C_{SPEC}$.
5. $t_{AW} = 2\,t_{CY} - t_{D3} - t_{r\phi2} - 120$nsec.
6. $t_{DW} = t_{CY} - t_{D3} - t_{r\phi2} - 150$nsec.
7. Data in must be stable for this period during DBIN $\cdot T_3$. Both t_{DS1} and t_{DS2} must be satisfied.
8. Ready signal must be stable for this period during T_2 or T_W. (Must be externally synchronized.)
9. Hold signal must be stable for this period during T_2 or T_W when entering hold mode, and during T_3, T_4, T_5 and T_{WH} when in hold mode. (Must be externally synchronized.)
10. Interrupt signal must be stable during this period of the last clock cycle of any instruction to be recognized on the following instruction. (External synchronization is not required.)
11. During halt mode only, timing is with respect to ϕ_1 falling edge.
12. This timing diagram shows timing relationships only, it does not represent any specific machine cycle.