

8080 MICROPROCESSOR

2. PROCESSOR TIMING

2-1. 8080 FUNCTIONAL PIN DEFINITION

The following describes the function of all of the 8080 I/O pins. Several of the descriptions refer to internal timing periods.

A₁₅-A₀ (output three-state)

ADDRESS BUS; the address bus provides the address to memory (up to 64K 8-bit words) or denotes the I/O device number for up to 256 input and 256 output devices. A₀ is the least significant address bit.

D₇-D₀ (input/output three-state)

DATA BUS; the data bus provides bidirectional communication between the CPU, memory, and I/O devices for instructions and data transfers. D₀ is the least significant bit.

SYNC (output)

SYNCHRONIZING SIGNAL; the SYNC pin provides a signal to indicate the beginning of each machine cycle.

DBIN (output)

DATA BUS IN; the DBIN signal indicates to external circuits that the data bus is in the input mode. This signal should be used to enable the gating of data onto the 8080 data bus from memory or I/O.

READY (input)

READY; the READY signal indicates to the 8080 that valid memory or input data is available on the 8080 data bus. This signal is used to synchronize the CPU with slower memory or I/O devices. If after sending an address out the 8080 does not receive a READY input, the 8080 will enter a WAIT state for as long as the READY line is low. (READY can also be used to single step the CPU.)

WAIT (output)

WAIT; the WAIT signal acknowledges that the CPU is in a WAIT state.

WR (output)

WRITE; the \overline{WR} signal is used for memory WRITE or I/O output control. The data on the data bus is stable while the \overline{WR} signal is active low ($\overline{WR} = 0$).

HOLD (input)

HOLD; the HOLD signal requests the CPU to enter the HOLD state. The HOLD state allows an external device to gain control of the 8080 address and data bus as soon as the 8080 has completed its use of these buses for the current machine cycle. It is recognized under the following conditions:

- the CPU is in the HALT state.
- the CPU is in the T₂ or T_W state and the READY signal is active.

As a result of entering the HOLD state the CPU ADDRESS BUS (A₁₅-A₀) and DATA BUS (D₇-D₀) will be in their high impedance state. The CPU acknowledges its state with the HOLD ACKNOWLEDGE (HLDA) pin.

HLDA (output)

HOLD ACKNOWLEDGE; the HLDA signal appears in response to the HOLD signal and indicates that the data and address bus will go to the high impedance state. The HLDA signal begins at:

- T₃ for READ memory or input.
- The Clock Period following T₃ for WRITE memory or OUTPUT operation.

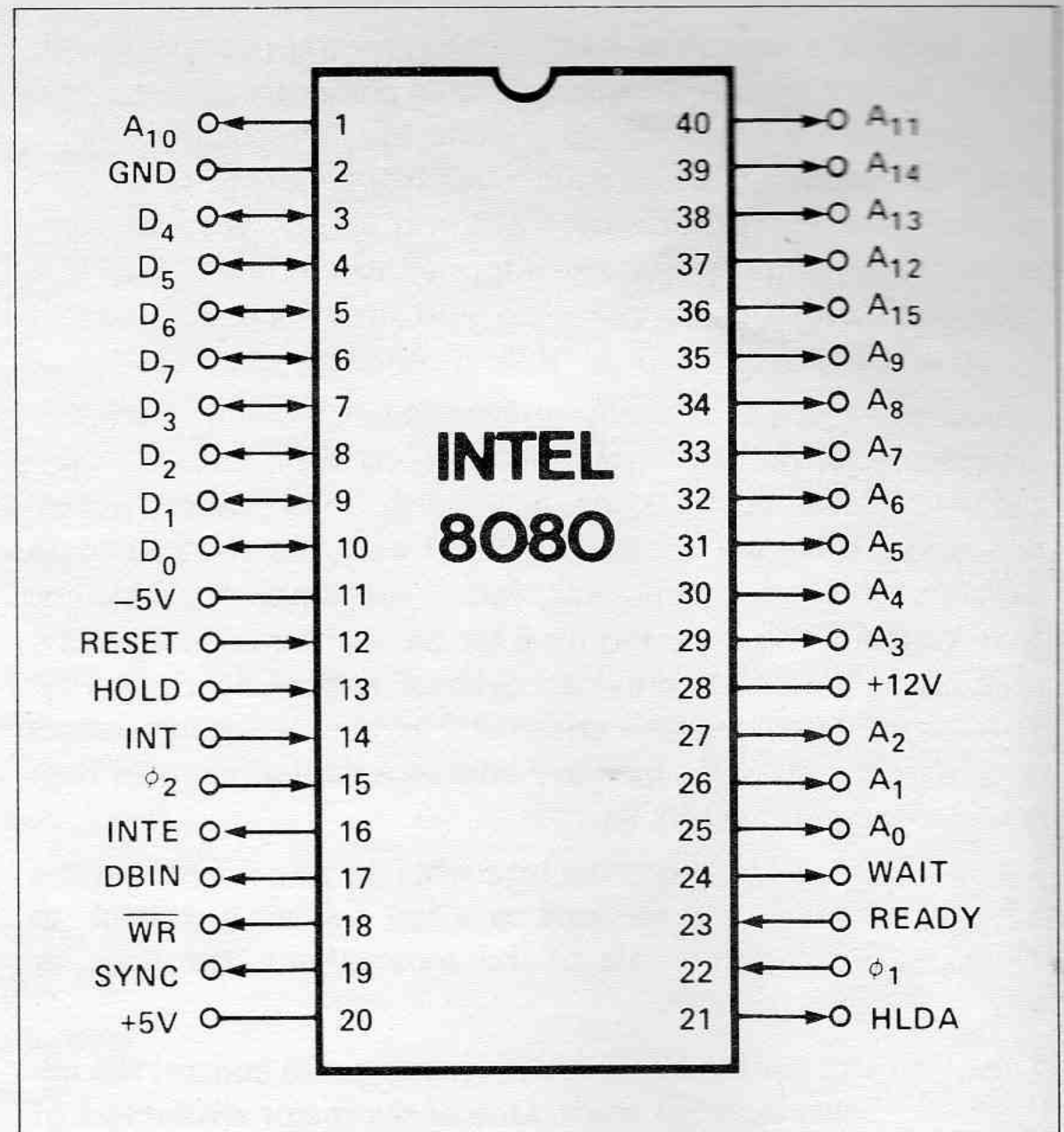


Figure 2. Pin Configuration

In either case, the HLDA signal appears after the rising edge of ϕ_1 and high impedance occurs after the rising edge of ϕ_2 .

INTE (output) [1]

INTERRUPT ENABLE; indicates the content of the internal interrupt enable flip/flop. This flip/flop may be set or reset by the Enable and Disable Interrupt instructions and inhibits interrupts from being accepted by the CPU when it is reset. It is automatically reset (disabling further interrupts) at time T₁ of the instruction fetch cycle (M1) when an interrupt is accepted and is also reset by the RESET signal.

INT (input)

INTERRUPT REQUEST; the CPU recognizes an interrupt request on this line at the end of the current instruction or while halted. If the CPU is in the HOLD state or if the Interrupt Enable flip/flop is reset it will not honor the request.

RESET (input)

RESET; while the RESET signal is activated, the content of the program counter is cleared. After RESET, the program will start at location 0 in memory. The INTE and HLDA flip/flops are also reset. Note that the flags, accumulator, stack pointer, and registers are not cleared.

V_{SS} Ground Reference. V_{CC} +5 ± 5% Volts.
 V_{DD} +12 ± 5% Volts. V_{BB} -5 ± 5% Volts (substrate bias).

Note 1: After the EI instruction, the CPU will accept interrupts on the second instruction following the EI. This is to allow proper processing of the RET instruction if an interrupt is pending after the service routine.