

8080 MICROPROCESSOR

2-3. STATUS INFORMATION

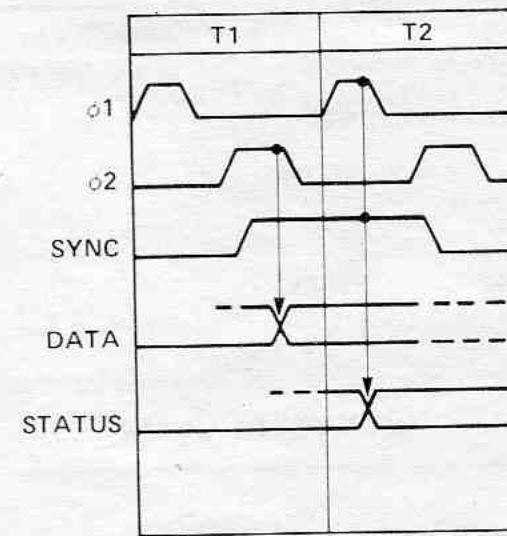
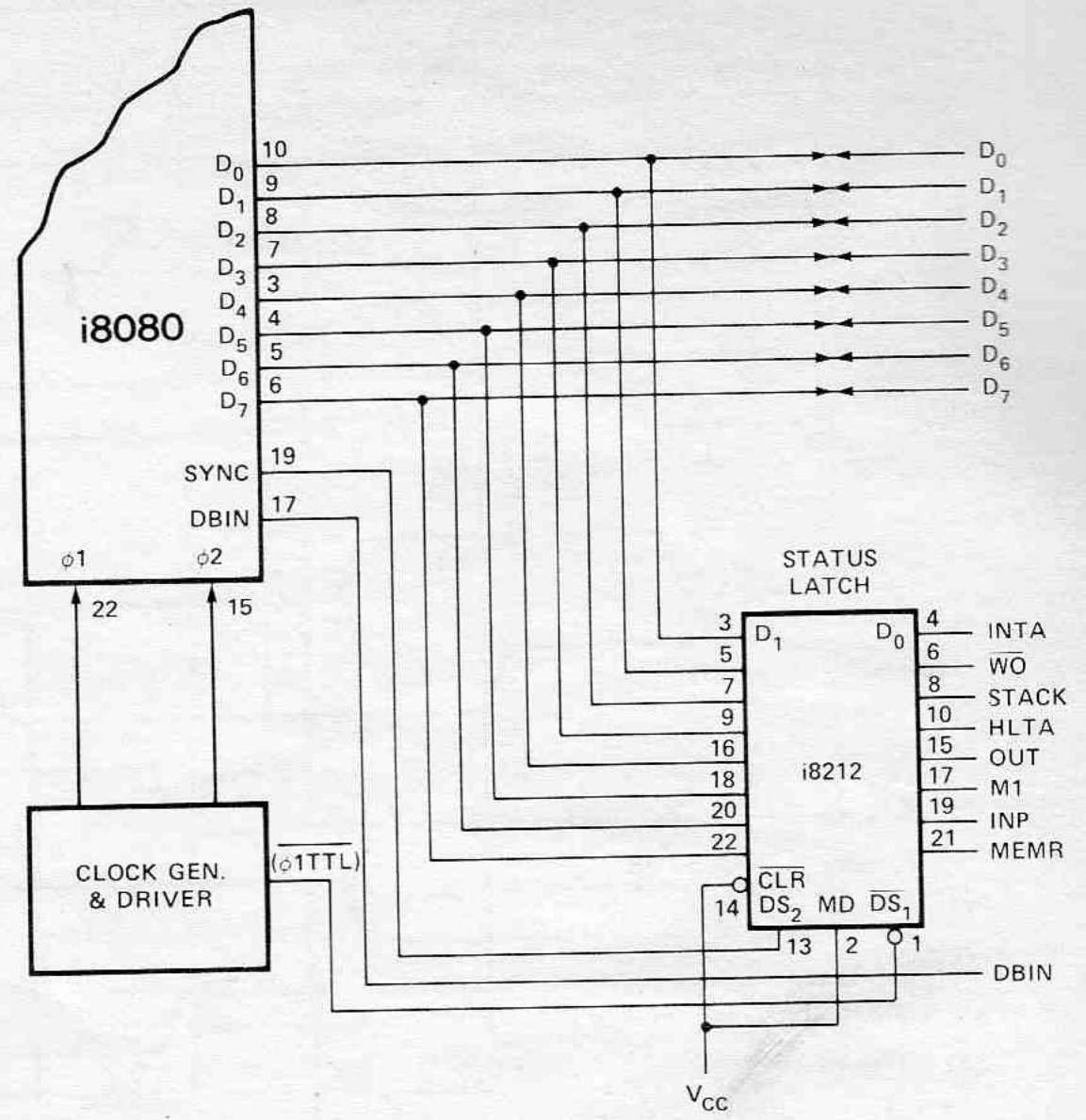
Instructions for the 8080 require from one to five machine cycles for complete execution. The 8080 sends out 8 bit of status information on the data bus at the beginning of each machine cycle (during SYNC time). The following table defines the status information.

STATUS INFORMATION DEFINITION

Symbols	Data Bus Bit	Definition
INTA*	D ₀	Acknowledge signal for INTERRUPT request. Signal should be used to gate a re-start instruction onto the data bus when DBIN is active.
\overline{WO}	D ₁	Indicates that the operation in the current machine cycle will be a WRITE memory or OUTPUT function ($\overline{WO} = 0$). Otherwise, a READ memory or INPUT operation will be executed.
STACK	D ₂	Indicates that the address bus holds the pushdown stack address from the Stack Pointer.
HLTA	D ₃	Acknowledge signal for HALT instruction.
OUT	D ₄	Indicates that the address bus contains the address of an output device and the data bus will contain the output data when WR is active.
M ₁	D ₅	Provides a signal to indicate that the CPU is in the fetch cycle for the first byte of an instruction.
INP*	D ₆	Indicates that the address bus contains the address of an input device and the input data should be placed on the data bus when DBIN is active.
MEMR*	D ₇	Designates that the data bus will be used for memory read data.

*These three status bits can be used to control the flow of data onto the 8080 data bus.

8080 STATUS LATCH



STATUS WORD CHART

DATA BUS BIT	STATUS INFORMATION	TYPE OF MACHINE CYCLE									
		①	②	③	④	⑤	⑥	⑦	⑧	⑨	⑩
D ₀	INTA	0	0	0	0	0	0	0	1	0	1
D ₁	\overline{WO}	1	1	0	1	0	1	0	1	1	1
D ₂	STACK	0	0	0	1	1	0	0	0	0	0
D ₃	HLTA	0	0	0	0	0	0	0	0	1	1
D ₄	OUT	0	0	0	0	0	0	1	0	0	0
D ₅	M ₁	1	0	0	0	0	0	0	1	0	1
D ₆	INP	0	0	0	0	0	1	0	0	0	0
D ₇	MEMR	1	1	0	1	0	0	0	0	1	0