3. PROCESSOR INSTRUCTION SET

3-1. COMPLETE FUNCTIONAL DEFINITION

The following pages present a detailed description of the complete 8080 Instruction Set.

Symbols	Meaning
<B2>	Second byte of the instruction
<B3>	Third byte of the instruction
r	One of the scratch pad register references: A, B, C, D, E, H, L
c	One of the following flag flip-flop references:

flag flip-flops.

Condition for True	
carry	— Overflow, underflow
zero	— Result is zero
sign	— MSB of result is "1"
parity	— Parity of result is even

M	Memory location indicated by the contents of registers H and L
( )	Contents of location or register
Λ	Logical product
∀	Exclusive "or"
V	Inclusive "or"
r_m	Bit m of register r
SP	Stack Pointer
PC	Program Counter
←	Is transferred to
XXX	A "don't care"
SSS	Source register for data
DDD	Destination register for data

Register # (SSS or DDD)	Register Name
000	B
001	C
010	D
011	E
100	H
101	L
110	Memory
111	ACC

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INSTRUCTION SET

Mnemonic	Bytes	Cycles	Description of Operation
MOV r_1, r_2	1	1	$(r_1) \leftarrow (r_2)$ Load register r_1 with the content of r_2. The content of r_2 remains unchanged.
MOV r, M	1	2	(r) ← (M) Load register r with the content of the memory location addressed by the contents of registers H and L.
MOV M, r	1	2	(M) ← (r) Load the memory location addressed by the contents of registers H and L with the content of register r.
MVI r <B_2>	2	2	(r) ← <B_2> Load byte two of the instruction into register r.
MVI M <B_2>	2	3	(M) ← <B_2> Load byte two of the instruction into the memory location addressed by the contents of registers H and L.