

8080 MICROPROCESSOR

Mnemonic	Bytes	Cycles	Description of Operation
RAL	1	1	$A_{m+1} \leftarrow A_m, A_0 \leftarrow (\text{carry}), (\text{carry}) \leftarrow A_7$ Rotate the content of Register A left one bit. Rotate the content of the carry flip-flop into A_0 . Rotate A_7 into the carry flip-flop.
RAR	1	1	$A_m \leftarrow A_{m+1}, A_7 \leftarrow (\text{carry}), (\text{carry}) \leftarrow A_0$ Rotate the content of register A right one bit. Rotate the content of the carry flip-flop into A_7 . Rotate A_0 into the carry flip-flop.
JMP <B ₂ > <B ₃ >	3	3	$(PC) \leftarrow \langle B_3 \rangle \langle B_2 \rangle$ Jump unconditionally to the instruction located in memory location addressed by byte two and byte three.
JC <B ₂ > <B ₃ >	3	3	If (Carry) = 1 $(PC) \leftarrow \langle B_3 \rangle \langle B_2 \rangle$ Otherwise $(PC) = (PC) + 3$
JNC <B ₂ > <B ₃ >	3	3	If (Carry) = 0 $(PC) \leftarrow \langle B_3 \rangle \langle B_2 \rangle$ Otherwise $(PC) = (PC) + 3$
JZ <B ₂ > <B ₃ >	3	3	If (Zero) = 1 $(PC) \leftarrow \langle B_3 \rangle \langle B_2 \rangle$ Otherwise $(PC) = (PC) + 3$
JNZ <B ₂ > <B ₃ >	3	3	If (Zero) = 0 $(PC) \leftarrow \langle B_3 \rangle \langle B_2 \rangle$ Otherwise $(PC) = (PC) + 3$
JP <B ₂ > <B ₃ >	3	3	If (Sign) = 0 $(PC) \leftarrow \langle B_3 \rangle \langle B_2 \rangle$ Otherwise $(PC) = (PC) + 3$
JM <B ₂ > <B ₃ >	3	3	If (Sign) = 1 $(PC) \leftarrow \langle B_3 \rangle \langle B_2 \rangle$ Otherwise $(PC) = (PC) + 3$
JPE <B ₂ > <B ₃ >	3	3	If (Parity) = 1 $(PC) \leftarrow \langle B_3 \rangle \langle B_2 \rangle$ Otherwise $(PC) = (PC) + 3$
JPO <B ₂ > <B ₃ >	3	3	If (Parity) = 0 $(PC) \leftarrow \langle B_3 \rangle \langle B_2 \rangle$ Otherwise $(PC) = (PC) + 3$
HLT	1	1	On receipt of the Halt Instruction, the activity of the processor is immediately suspended in the STOPPED state. The content of all registers and memory is unchanged and the PC has been updated.
CALL <B ₂ > <B ₃ >	3	5	$[SP - 1] [SP - 2] \leftarrow (PC), (SP) = (SP) - 2$ $(PC) \leftarrow \langle B_3 \rangle \langle B_2 \rangle$ Transfer the content of PC to the pushdown stack in memory addressed by the register SP. The content of SP is decremented by two. Jump unconditionally to the instruction located in memory location addressed by byte two and byte three of the instruction.
CC <B ₂ > <B ₃ >	3	3/5	If (carry) = 1 $[SP - 1] [SP - 2] \leftarrow PC,$ $(SP) = (SP) - 2, (PC) \leftarrow \langle B_3 \rangle \langle B_2 \rangle;$ otherwise $(PC) = (PC) + 3$
CNC <B ₂ > <B ₃ >	3	3/5	If (carry) = 0 $[SP - 1] [SP - 2] \leftarrow PC,$ $(SP) = (SP) - 2, (PC) \leftarrow \langle B_3 \rangle \langle B_2 \rangle;$ otherwise $(PC) = (PC) + 3$
CZ <B ₂ > <B ₃ >	3	3/5	If (zero) = 1 $[SP - 1] [SP - 2] \leftarrow PC,$ $(SP) = (SP) - 2, (PC) \leftarrow \langle B_3 \rangle \langle B_2 \rangle;$ otherwise $(PC) = (PC) + 3$
CNZ <B ₂ > <B ₃ >	3	3/5	If (zero) = 0 $[SP - 1] [SP - 2] \leftarrow PC,$ $(SP) = (SP) - 2, (PC) \leftarrow \langle B_3 \rangle \langle B_2 \rangle;$ otherwise $(PC) = (PC) + 3$
CP <B ₂ > <B ₃ >	3	3/5	If (sign) = 0 $[SP - 1] [SP - 2] \leftarrow PC,$ $(SP) = (SP) - 2, (PC) \leftarrow \langle B_3 \rangle \langle B_2 \rangle;$ otherwise $(PC) = (PC) + 3$