| Mnemonic | Bytes | Cycles | Description of Operation |
|---|---|---|---|
| CM<br><$B_2$><br><$B_3$> | 3 | 3/5 | If (sign) = 1 [SP − 1] [SP − 2] ← PC,<br>(SP) = (SP) − 2, (PC) ← <$B_3$> <$B_2$>;<br>otherwise (PC) = (PC) + 3 |
| CPE<br><$B_2$><br><$B_3$> | 3 | 3/5 | If (parity) = 1 [SP − 1] [SP − 2] ← PC,<br>(SP) = (SP) − 2, (PC) ← <$B_3$> <$B_2$>;<br>otherwise (PC) = (PC) + 3 |
| CPO<br><$B_2$><br><$B_3$> | 3 | 3/5 | If (parity) = 0 [SP − 1] [SP − 2] ← PC,<br>(SP) = (SP) − 2, (PC) ← <$B_3$> <$B_2$>;<br>otherwise (PC) = (PC) + 3 |
| RET | 1 | 3 | (PC) ← [SP] [SP + 1] (SP) = (SP) + 2. Return to the instruction in the memory location addressed by the last values shifted into the pushdown stack addressed by SP.<br>The content of SP is incremented by two. |
| RC | 1 | 1/3 | If (carry) = 1 (PC) ← [SP], [SP + 1],<br>(SP) = (SP) + 2;<br>otherwise (PC) = (PC) + 1 |
| RNC | 1 | 1/3 | If (carry) = 0 (PC) ← [SP], [SP + 1],<br>(SP) = (SP) + 2;<br>otherwise (PC) = (PC) + 1 |
| RZ | 1 | 1/3 | If (zero) = 1 (PC) ← [SP], [SP + 1],<br>(SP) = (SP) + 2;<br>otherwise (PC) = (PC) + 1 |
| RNZ | 1 | 1/3 | If (zero) = 0 (PC) ← [SP], [SP + 1],<br>(SP) = (SP) + 2;<br>otherwise (PC) = (PC) + 1 |
| RP | 1 | 1/3 | If (sign) = 0 (PC) ← [SP], [SP + 1],<br>(SP) = (SP) + 2;<br>otherwise (PC) = (PC) + 1 |
| RM | 1 | 1/3 | If (sign) = 1 (PC) ← [SP], [SP + 1],<br>(SP) = (SP) + 2;<br>otherwise (PC) = (PC) + 1 |
| RPE | 1 | 1/3 | If (parity) = 1 (PC) ← [SP], [SP + 1],<br>(SP) = (SP) + 2;<br>otherwise (PC) = (PC) + 1 |
| RPO | 1 | 1/3 | If (parity) = 0 (PC) ← [SP], [SP + 1],<br>(SP) = (SP) + 2;<br>otherwise (PC) = (PC) + 1 |
| RST | 1 | 3 | [SP − 1] [SP − 2] ← (PC),<br>(SP) = (SP) − 2<br>(PC) ← (00000000 00AAA000) |
| IN<br><$B_2$> | 2 | 3 | (A) ← (Input data)<br>At $T_1$ time of third cycle, byte two of the instruction, which denotes the I/O device number, is sent to the I/O device through the address lines*, and the INP status information, instead of MEMR, is sent out at sync time. New data for the accumulator is loaded from the data bus when DBIN control signal is active. The condition flip-flops are not affected. |
| OUT<br><$B_2$> | 2 | 3 | (Output data) ← (A)<br>At $T_1$ time of the third cycle, byte two of the instruction, which denotes the I/O device number, is sent to the I/O device through the address lines*, and the OUT status information is sent out at sync time. The content of the accumulator is made available on the data bus when the $\overline{WR}$ control signal is 0. |
| LXI B<br><$B_2$><br><$B_3$> | 3 | 3 | (C) ← <$B_2$>; (B) ← <$B_3$><br>Load byte two of the instruction into C. Load byte three of the instruction into B. |
| LXI D<br><$B_2$><br><$B_3$> | 3 | 3 | (E) ← <$B_2$>, (D) ← <$B_3$><br>Load byte two of the instruction into E. Load byte 3 of the instruction into D. |
| LXI H<br><$B_2$><br><$B_3$> | 3 | 3 | (L) ← <$B_2$>, (H) ← <$B_3$><br>Load byte two of the instruction into L. Load byte three of the instruction into H. |

*The device address appears on $A_7 - A_0$ and $A_{15} - A_8$